LESSON PLAN (B.TECH)

Verilog HDL

Subject Code : 17EC53 **CIE Marks : 40**
No. of lecture Hrs / Week : 04 **Exam Hrs : 03**
Total no. of lecture Hrs : 50 **SEE Marks : 60**
Faculty : CHIRANJEEVI .G. N

Chapter Title	Class No.	Topics to be covered (in detail)	% Portions covered	
			Reference Chapter	Cumulative
PART A				
Module-1	1,2	**Overview of Digital Design with Verilog HDL**	1	10
	3,4,5	Evolution of CAD, emergence of HDLs, typical HDL-flow		
	6,7	why Verilog HDL?, trends in HDLs.		
	8	**Hierarchical Modeling Concepts** Top-down and bottom-up design methodology		
	9,10	differences between modules and module instances, parts of a simulation, design block, stimulus block.		
Module-2	11-15	**Basic Concepts** Lexical conventions, data types, system tasks, compiler directives.	2	25
	16-20	**Modules and Ports** Module definition, port declaration, connecting ports, hierarchical name referencing		
Module-3	21-23	**Gate-Level Modeling** Modeling using basic Verilog gate primitives, description of and/or and buf/not type gates,	3	39
	24	rise, fall and turn-off delays, min, max, and typical delays.		
	25,26	**Dataflow Modeling** Continuous assignments, delay specification, expressions,		

	27-30	operators, operands, operator types.		
Module-4	31,32	**Behavioral Modeling** Structured procedures, initial and always,	4	49
	33,34	blocking and non-blocking statements		
	35,36	delay control, generate statement		
	37,38	event control, conditional statements		
	39,40	Multiway branching, loops, sequential and parallel blocks.		
PART – B				
Module-5	41	**Introduction to VHDL:**	5	62
	42	Why use VHDL?,		
	43-46	Shortcomings, Using VHDL for Design Synthesis,		
	47-50	Design tool flow, Font conventions.		

TEXT BOOKS

Reference Books:

1. Samir Palnitkar, "Verilog HDL: A Guide to Digital Design and Synthesis", Pearson Education, Second Edition.

2. Kevin Skahill, "VHDL for Programmable Logic", PHI/Pearson education, 2006. "

Note :

1. Two quizzes and three assignments are mandatory.

2. Quiz no.1 will be conducted in week 4 and quiz no. 2 will be conducted in the 9th week.

3. **Portions for T1**: Unit 1 + Unit 2 + Unit 3

4. **Portions for T2**: Unit 3(excluding T1 portions) + Unit 4 + Unit 5

5. **Portions for T3**: Unit 6 + Unit 7

6. **Submission Deadline for Assignment 1**: SEP, 2019

7. **Submission Deadline for Assignment 2**: OCT, 2019

8. **Submission Deadline for Assignment 3**: NOV ,2019