15CS32: Analog and Digital Electronics

Question Bank

MODULE I

1. Explain the construction, working and characteristics of N-channel MOSFET with neat sketches.
2. What are the differences between BJTs and FETs?
3. Give the comparison between JFETs and MOSFETs.
4. Mention the merits and demerits of IGBT.
5. Write the advantages of MOSFET over JFET.
6. What are the differences between JFETs and MOSFETs?
7. Explain the construction, principle and working of n channel JFET.
8. Explain with neat sketches the operation of JFET along with its characteristic curves.
9. Explain the V-I characteristics of n-channel JFET and define various conditions.
10. Explain the construction and working of n channel depletion mode MOSFET.
11. Explain the construction, working and characteristics of n channel Enhancement mode MOSFET with neat sketches.
12. Explain the working of an CMOS inverter.
13. Briefly discuss the basic operation of CMOS inverter with a neat diagram. Mention any two advantages.
14. Explain with neat sketches the operation, characteristics and parameters of n channel depletion type MOSFET.
15. Explain with neat sketches the operation and characteristics of N-channel DE-MOSFET.
16. With the help of a neat figure explain the construction and characteristics of N channel depletion MOSFET.
17. Find the values of $V_d$ and $V_c$ for the circuit shown, Assume $\beta=100, V_{BE}=0.7V$, saturation drain current of JFET= -10 mA and pinch off voltage = -5V.
18. Calculate the value of operating point for the circuit shown in Fig. Q2 (b) given that threshold voltage for the MOSFET is 2V and ID (ON) = 6 mA for VGS(ON) = 5 V.

19. Fig Q2(c) shows a biasing configuration using DE-MOSFET. Given that the saturation drain current is 8 mA and pinch off voltage is -5V. Determine the drain source voltage, drain current and gate source voltage.

20. What are the necessary conditions for loop gain and phase shift for sustained oscillations according to Barkhausen criterion?

21. Explain the working of an Astable Multivibrator using 555 timer with circuit diagram and relevant waveforms.

22. Explain the working of RC Low Pass and RC High Pass circuit.

23. Briefly explain the characteristics of ideal OP-AMP and compare with practical OP-AMP.
24. With relevant formulas, neat diagram and waveform explain OPAMP Schmitt trigger
25. Explain the working of an OPAMP window comparator with circuit diagram
26. Explain lead and lag type phase shifter
27. What should be the slew rate chosen for an OPAMP with an inverting amplifier configuration with gain of 10 when input is a sinusoidal signal with peak to peak value of 2V and highest frequency expected is 50Hz?
28. Discuss briefly the working operation of astable Multivibrator using IC555 timer
29. What are active filters using op-amp? Explain first order low pass and high pass filters with gain.
30. Explain with circuit the working operation of instrumentation amplifier.
31. Calculate the values of R1, R2, C1, C2 and R3. If the filter had a cut off frequency of 10 kHz factor of 0.707 and input impedance not less than 10 Kohm for the Fig. shown which has a second order low pass filter built around a single operational amplifier.

![Diagram]

32. With a neat figure, explain the operation of a peak detector circuit using OPAMP
33. With neat figure and relevant waveforms explain the working of relaxation oscillator circuit using OPAMP
34. Define the following as referred to OPAMP
   i) CMRR ii) PSRR iii) Slew Rate iv) Band Width v) Open Loop gain
35. List and explain the performance parameters of operational amplifiers
36. Explain the working of comparator as zero crossing detectors
37. For the relaxation oscillator circuit shown in Fig Q.8(c), determine the heat to heat amplitude and frequency of the square wave output given that the saturation output voltage of the OPAMP is +/-12.5V at power supply voltages of +/-15V
38. Explain with neat diagram: i) Peak detector circuit ii) Absolute value circuit and their working
39. Explain with neat diagram: i) Current to voltage converter ii) Voltage to current converter and their working
40. Explain the working of monostable multivibrator with a neat diagram
41. Explain RC low pass circuit and discuss the behavior of this circuit towards step and pulse inputs
42. Write a note on Barkhausen criterion
43. Explain the various type of multivibrators and their applications
44. Obtain the expression for the time period $T_t$ at the base of the transistor in case of wave shaping circuits.
45. Discuss the requirements of a good instrumentation amplifier
46. Explain the various electrical characteristics of an operational amplifier which are generally present in a data sheet.
47. Fig Q.8.b) shows dual input balanced output and differential amplifier configuration. Assuming silicon transistor with $h_{ie}=2.8 \, K\Omega$, calculate i) operating point values ii) differential mode gain iii) common mode gain iv) CMRR v) Output if $V_s1=70 \, mV$ peak to peak at 1 KHz vi) Output if $V_s2=40 \, mV$ peak to peak at 1 KHz
MODULE II

1. Differentiate analog and digital signals. Define period, frequency and duty cycle of a digital signal. Prove that duty cycle of a symmetrical signal is 50%.

2. An asymmetrical signal waveform is HIGH for 2 msec and LOW for 5 msec. Find the frequency and duty cycle of the waveform.

3. Define rise time, fall time in a digital waveform. What is the value of high duty cycle (duty cycle if the frequency of a digital waveform is 5 MHz and the width of the positive pulse is 0.05 µs?

4. What are logic gates? State and prove De Morgan’s Theorems.

5. State De Morgan’s Theorems for 2 variables. Prove using perfect induction

6. Write the truth table of a logic circuit having 3 inputs A, B and C. The output Y=A'BC+ABC. Also simplify the expression using Boolean algebra

7. Name the Universal gates. Realize basic gates using NAND gates.

8. Realize ((A+B)’.C) using only NAND gates.

9. Implement the following logic using (i) NAND gates only (ii) NOR gates only ( (A+B).C)’.D

10. Implement AB +C’D’ with only 3 NAND gates. Draw logic diagram also. Assume inverted input is available.

11. Implement the following function using Universal gates only ( (A+B)’.C)’.D

12. Draw logic circuit whose Boolean equation is Y=(A+B)’+C’, use only NAND gates

13. Describe positive and negative logic. List the equivalences between them

14. Describe positive and negative logic. Prove positive OR logic is equal to negative AND logic

15. Write a Verilog HDL code using structural model for two-input AND gate and prepare test bench to simulate the circuit. Draw the timing diagram generated by simulating the Verilog code. Assume 20 ns holding time of each input combination.

16. Find the minimal SOP of the following Boolean functions using K-Maps:

   a) \( f(a, b, c, d) = \sum m(6, 7, 9, 10, 13) + d(1, 4, 5, 11) \)

   b) \( f(w, x, y, z) = \sum \pi m(1, 2, 3, 4, 9, 10) + d(0, 1, 4, 15) \)
17. Give Sum of Product and Product of Sum circuit for
   \[ f(a, b, c, d) = \sum m(6, 8, 9, 10, 11, 12, 13, 14, 15) \]

18. A digital system is to be designed in which the month of the year is given as input is four bit form. The month January is represented as '0000' February '0001' and so on. The output of the system should be '1' corresponding to the input of the month containing 31 days or otherwise it is '0' consider the excess numbers in the input beyond '1011' as don't care conditions for system of four variables (A, B, C, D) find the following:
   a) Boolean expression in \( \Sigma m \) and \( \Pi m \) form
   b) Write the truth table
   c) Using K-map, simplify the Boolean expression of canonical minterm form
   d) Implement the simplified equation using NAND - NAND gates

19. Using K-Map technique simplify
   \[ f(a, b, c, d) = \sum (1, 2, 4, 5, 6, 8, 9, 11, 15) + dc(3, 7, 13) \]

20. Simplify the Boolean function \( A, B, C, D = \sum m(1, 3, 5, 7, 8, 10, 12, 14) \) by using Karnaugh map method and realize the logic circuit using only NAND gates.

21. Draw Karnaugh map of
   \[ Y = F (A, B, C, D) = \Pi M (0, 1, 2, 4, 5, 10), d (8, 9, 11, 12, 13, 15) \]
   and get the simplified POS form

22. Find the minimal SOP and minimal POS of the following Boolean function using K-map
   \[ f(a, b, c, d) = \sum m(6, 7, 9, 10, 13) + d(1, 4, 5, 11) \]

23. Using Q-M method, simplify the expressions \( f (A, B, C, D) = \sum m (0, 3, 5, 6, 7, 11, 14) \).
   Write the gate diagram for the simplified expression using NAND - NAND gates.

24. Simplify \( f(A, B, C, D) = \sum m(0, 1, 2, 3, 10, 11, 12, 13, 14, 15) \) using Quine-McClusky method.

25. Find the essential prime implicants for the Boolean Expression by using QuineMcClusky method.
   \[ f(A, B, C, D) = \sum m(1, 3, 6, 7, 8, 9, 10, 12, 13, 14) \]

26. Using Quine McClusky method, simplify
   \[ f(w, x, y, z) = \sum (0, 1, 3, 4, 7, 12, 14, 15) \]

27. Get simplified expression of \( Y = F (A, B, C, D) = \sum m (2, 3, 7, 9, 11, 13) + d (1, 10, 15) \) using Quine-McClusky method.

28. Using Quine McClusky method, simplify
29. What are static hazards? How to design a hazard free circuit? Explain with an example.
30. Does the circuit in figure experience hazard? If so, verify the same with timing diagram

31. Write a note on static hazards
MODULE III

1. Differentiate between PROM, PAL, PLA
2. Explain the Implementation of Full adder using PLA
3. Design and implement BCD to excess-3 code converter using four 8:1 multiplexers.
   Take MSB 'A' as map entered variable (input variable) 'BCD' lines as select lines, assuming f(A, B, C, D) as BCD input.
4. Realize a logic circuit for Octal to binary encoder. (06 Marks)
5. Draw the PLA circuit and realize the Boolean functions:
   X = A'B'C + AB'C' + B'C, Y = A'B'C + AB'C', Z = B'C
6. Give the HDL implementation of 2:1 MUX.
7. Explain 4 - bit magnitude comparator.
8. Realize a full adder using a 3:8 Decoder
9. Write a 4:1 MUX Verilog Program using conditional assign and case statement
10. Implement the following Boolean Functions using a PLA
    F1 = \( \sum \{0, 1, 4, 6\} \) F2 = \( \sum \{2, 3, 4, 6, 7\} \),
    F3 = \( \sum \{0, 1, 2, 6\} \) F4 = \( \sum \{2, 3, 5, 6, 7\} \)
11. Realise Octal to Binary Encoder
12. Design 7 Segment Decoder Using PLA
13. Design a 16 to 1 MUX using two 8 to 1 MUX and one 2 To 1 MUX
14. Implement Boolean Function expressed by the POS function
    F(a, b, c, d) = \( \pi \{1, 2, 5, 6, 9, 12\} \) using 8:1 MUX
15. What is a multiplexer? Design a 4-to-1 multiplexer using logic gates, write the truth table and explain its work principle.
16. Describe the working principle of 3:8 decoder. Design a circuit that realizes the following functions using a 3 to 8 decoder and multi-input OR gates.
    F1 (A, B, C) = \( \sum m \{1, 3, 7\} \), F2 (A, B, C) = \( \sum m \{2, 3, 5\} \)
17. What is a magnitude comparator? Design one bit comparator and write the truth table, logic circuit using basic gates.
18. How does Programmable Logic Arrays (PLA) differ from Programmable Array Logic (PAL)?
19. Differentiate between combinational circuit and sequential circuits
22. Explain the characteristics of an ideal clock.
23. Draw the logic diagram of clock D - flip/flop write its truth table and characteristic equation, state diagram and excitation table, what is the drawback of JK flip/flop.
24. With the help of neat diagram, explain the working of edge triggered JK flip flop.
    Write the state diagram and excitation table.
25. Draw the logic diagram, truth table and timing diagram for edge-triggered D-flip flop.
26. With a neat logic diagram and truth table, explain the working of JK Master-Slave Flip-Flop along with its implementation using NAND gates.
27. What is switch contact bounce? Explain the working principle of a simple RS latch debounce circuit.
MODULE IV

1. Show how a D Flip Flop can be converted to a JK Flip Flop.
2. Show how a SR flip/flop can be converted into T - flip/flop.
3. Write the state table and state diagram for the figure shown.

4. Analyze the behavior of the sequential circuit shown in Figure and draw the state table and state transition diagram.

5. Write the state table and state diagram for the circuit shown in Fig.Q4(c).

7. Write Verilog code for positive edge triggered D Flip Flop.
8. Write a note on classification of registers
9. What is a shift register? Draw the logic diagram of a 4 bit serial in serial out (SISO) shift register using negative edge triggered JK or D flip-flops and explain its operation with the waveform to shift the binary number 1010 into the register.
10. Explain with logic diagram the use of 8-bit SISO shift register in serial addition of two 8-bit numbers.
11. With neat timing diagram, explain the working of 4 bit SISO register
12. With neat timing diagram, explain the working of 4 bit serial-in serial-out shift register (SISO) register. For explanation, construct 4 bit shift register using JK Flip flops.
13. Using positive edge triggered D flip-flops, draw logic diagram for a 4-bit parallel-in serial-out (PISO) shift register. Explain its working to load 1001 into it and shift the same.
14. How long will it take to shift an 4 bit number into 4 bit PISO shift register that operates at clock frequency of 5 MHz. Also, what is the time required to extract 4-bit number from PISO operates at 5 MHz clock?
15. Using negative edge triggered JK flip-flops, draw the logic diagram for a 4-bit serial-in serial-out (SISO) shift register. Draw the waveform to shift the binary number 1010 into this register. Also draw the waveforms for four clock transitions when J=K=0 (assuming the register has stored 1010 in it)
16. How long will it take to shift the hexadecimal number ‘AB’ into the 54/74164(SIPO) if 5 MHz clock is connected to it? Also mention the time required to extract an 8 bit number from the same register?
17. With neat diagram, explain a 4 bit universal shift register
18. Explain the working of mod-4 ring counter.
19. With neat diagram, explain how 7495 can be connected to function as switched tail counter
20. Explain with neat diagram, how shift register can be applied for serial addition.
21. Write Verilog code for Johnson Counter
22. Write Verilog code for Switched Tail Counter using always and assign statement.
23. Write Verilog HDL code for 4-bit SIPO shift register when all the flip-flop outputs are available externally.
24. Write Verilog code for a) Switched Tail Counter b) Shift register of 5-bits constructed using D Flip flops
MODULE V

1. Write the comparisons between synchronous and asynchronous counters.
2. What are asynchronous and synchronous counters? With a neat block diagram, output waveform and truth table, explain a 3-bit binary ripple counter constructed using negative edge triggered JK flip-flops.
3. With the help of neat block diagram and timing diagram, explain the working of a Mod-16 ripple counter constructed using positive edge triggered JK flip-flops.
4. List any two drawbacks of asynchronous counter. What is the clock frequency in a 3-bit counter, if the clock period of the waveform at last flip-flop is 24 us?
5. A 4 bit binary asynchronous counter is connected with a clock of 500 KHz frequency. Find the time period of the waveform at the output of the first and the last JK Flip Flop.
6. With the help of neat block diagram and timing diagram, explain the working of a mod-16 ripple counter constructed using the edge triggered JK flip/flop.
7. Design asynchronous counter for sequence 0 ~ 4 ~ 1 ~ 2 ~ 6 ~ 0 ~ 4, using SR flip-flop.
8. Design MOD-6 Synchronous up counter using JK FF.
9. Design a synchronous counter mod-6 counter using JK flip-flops waveform at the output of the first and the last JK Flip Flop.
11. Design a self-correcting Mod-5 synchronous down counter using JK flip-flops. Assume 100 as the next state for all the unused states.
12. Design a mod-5 counter using JK flip-flops having the feature that if an unused state appears, the counter will reset to 000 at the next clock pulse.
13. What do you mean by lockout condition in counters? Using JK FFs design self-correcting MOD-6 Counter.
14. Design mod-12 counter using IC 7493
15. Design a) a divide by 78 counter using IC 7492 and 7493 b)modulo 120 counter using7490 and 7492
16. Explain digital clock with a block diagram.
17. Discuss the two drawbacks of resistive divider used in converting digital input to analog input. Draw the schematic for a 4 bit binary ladder and explain how the digital to analog conversion is achieved using it.
18. What is binary ladder? Explain the binary ladder with a digital input of 1000.
19. What is accuracy and resolution of the D/A converter? What is the resolution of a 12 bit D/A converter which binary ladder? If the full scale output is +10 V, what is the resolution in volts?
20. With neat circuit diagram, explain the working of R-2R ladder DAC
21. With a neat diagram, explain the working of a 4-bit D/A converter.
22. What is the accuracy and resolution of an 8-bit D/A converter? Find the resolution and accuracy of the same if the full scale output is +10V.
23. Discuss the working of following A/D converters:
   a) Successive approximation A/D.
   b) Counter type A/D.
24. Using schematic block diagram, briefly explain counter type ADC
25. A counter Type ADC is connected to a 7 MHz clock. Find the average conversion time the maximum conversion rate.
27. Explain the working of ADC
28. Calculate conversion time for 10 bit ADC operating at 5 MHz clock
29. Explain with logic diagram a 3 bit simultaneous A/D converter
30. Explain with neat diagram single slope A/D converter
31. With a neat circuit diagram, explain parallel ADC.
32. Explain a neat diagram, explain Successive approximation A/D converter
33. With a neat diagram, explain Counter method of A/D conversion.
34. Write a note on
35. a) Binary ladder   b) Differences between A/D and D/A converters