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Hosur road, 1km before Electronic City, Bengaluru -100

Department of Electronics and Communication

VLSI Design and Embedded Systems

INTERNAL ASSESSMENT TEST 2

Date : 03/04/2017	Marks: **40**
Subject & Code : **VLSI Testing – 16EVE22**	Specialization : VLSI & EMB
Name of faculty : **Prof. Ananda M**	Time : 8:30am -10:00am

		Note: Answer FIVE full questions, selecting any ONE full question from each part.	**Marks**
		PART 1	
1		List test Generation Techniques for Combinational circuit and explain Fault Matrix method?	**8**
2		What is D-Algorithm? List the types of Cubes? Write the Singular Cubes and Propagation D-cube for two input Nor Gate?	**8**
		PART 2	
3		Explain the basic principle of Path Sensitization method to detect the fault in the circuit?	**8**
4		What is Primitive D-cube of a fault? Write Pdcf for all single stuck-at faults for the three-input NAND gate?	**8**
		PART 3	
5		What is BIST? Explain the Partitioning of a circuit for autonomous testing with an Example ?	**8**
6		What is BILBO? with Logic diagram of a BILBO explain BILBO-based BIST Architecture ?	**8**
		PART 4	
7		Explain D-algorithm method to generate a test for a given fault with the test generation process steps for detecting α(s-a-1) fault in Figure 7 below.	**8**
8		What is PODEM? With steps Illustrate the application of PODEM by deriving a test for fault l s-a-1 in the circuit shown in Figure 8 below	**8**
		PART 5	
9		Explain the basic principal of Boolean Difference with examples.	**8**
10		Explain the compression techniques for Output Response Analysis.	**8**

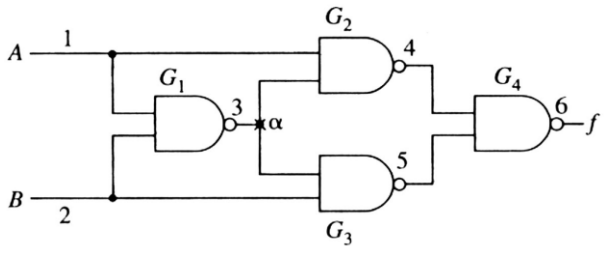

Figure 7 for Question 7

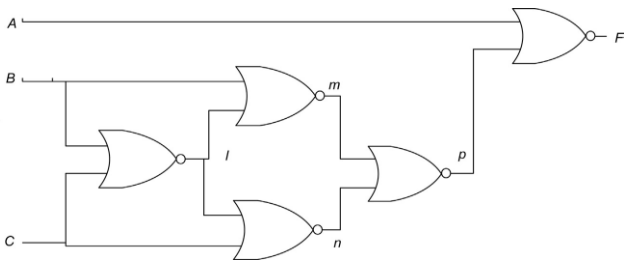

Figure 8 for Question 8

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SCHEME AND SOLUTION
SECOND INTERNAL TEST

Q.No	Note: Answer FIVE full questions, selecting any ONE full question from each part.	Marks
	PART 1	
(1)	Test Generation Techniques for Combinational circuit- 4 types-2 marks→ refer Text 1 Explaining the Fault Matrix method with circuit and truth table- 6marks → refer Text 1 Total= 2+6=8	**8 marks**
(2)	D-Algorithm – definition→ 2 marks→ refer Text 1 List the types of Cubes → 1 marks→refer Text 1 Writing the Singular Cubes and Propagation D-cube for two input Nor Gate: 5 marks → refer slides. Total= 2+1+5=8	**8 marks**
	PART-2	
(3)	The basic principle of Path Sensitization method to detect the fault in the circuit : Text 1→ Explanation 2 marks Circuit diagram : 2marks and 6 steps→4 marks Text 1 Total= 2+2+4 =8	**8 marks**
(4)	Primitive D-cube of a fault definition→ 2 marks→ Text 1 Writing Pdcf for all single stuck-at faults for the three-input NAND gate Circuit diagram →2 marks, explanation→ 4 marks Total= 2+2+4 =8	**8 marks**
	PART 3	
(5)	BIST definition- 2 marks → Text1 The Partitioning of a circuit for autonomous testing with an Example Circuit diagram → 3 marks and explanation→3 marks Total= 2+3+3=8	**8 marks**
(6)	BILBO definition → 2 marks→ Text1 Logic diagram of a BILBO → 3 marks Explaining BILBO-based BIST→ 3 marks Total= 2+3+3=8 marks	**8 marks**
	PART 4	

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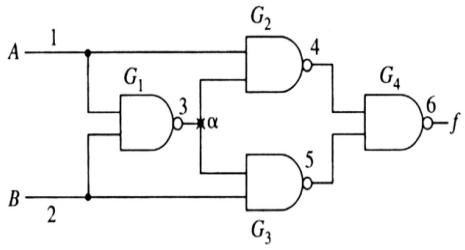
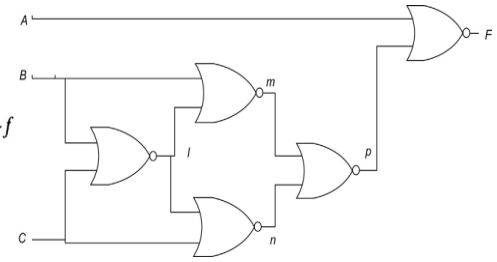
(7)	D-algorithm method to generate a test for a given fault with the test generation process steps for detecting α(s-a-1) fault in Figure 7 below.  Figure 7 for Question 7  Figure 8 for Question 8 Rewriting the circuit diagram Figure: →2 marks six steps for solving the circuit→ 6 marks Total= 2+4=8	**8 marks**
(8)	PODEM definition → 2 marks → Text1 Rewriting the circuit diagram Figure: → 2 marks With steps Illustrate the application of PODEM by deriving a test for fault l s-a-1 in the circuit shown in Figure 8 → 4 marks Total= 2+2+4=8	**8marks**
	PART 5	
(9)	The basic principal of Boolean Difference with examples →Explanation with equations → 4+4 marks Total= 4+4=8	**8 marks**
(10)	The compression techniques for Output Response Analysis 3 techniques →1 mark (1)Transition count explanation →1 marks (2) Syndrome →2 marks (3) Signature Analysis → Block diagram → 2 marks Explanation →2 marks Total=1+1+2+2+2=8	**8 marks**

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