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PESIT Bangalore South Campus

Hosur road, 1km before Electronic City, Bengaluru -100

Department of Electronics and Communication

VLSI Design and Embedded Systems

INTERNAL ASSESSMENT TEST 1

Date : 04/03/2017			Marks: **40**
Subject & Code : **RTOS – 16EVE24**			Specialization :VLSI & EMB
Name of faculty : **Prof. Ananda M**			Time : 11:30am -1:00pm
Note: Answer FIVE full questions, selecting any ONE full question from each part.			**Marks**
PART 1			
1		What is Deadline and Define RM LUB with relevant question	**8**
2		Explain two service feasibility testing by examination.	**8**
PART 2			
3		Explain the relationship between sufficient and N&S feasibility test.	**8**
4		With two-service examples used derive RM LUB for case1.	**8**
PART 3			
5		Compare the relationship of T2 and T1 for case1 and case 2	**8**
6		Derive an expression for RM LUB mathematically.	**8**
PART 4			
7		Explain two algorithms for determination of N&S feasibility testing with RM policy.	**8**
8		Explain RM policy for overload scenario and cascading overload scenario.	**8**
PART 5			
9		Explain the Worst-Case Execution Time (WCET) with relevant equation.	**8**
10		Write the overlapping definitions and also the overlapping conditions for CPU time	**8**

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SCHEME AND SOLUTION
SECOND INTERNAL TEST

QNo.	Note: Answer FIVE full questions, selecting any ONE full question from each part.	Marks
	PART 1	
(1)	Deadline definition →2marks → Text1 Define RM LUB with relevant question → 6 marks → refer Text 1 Total= 2+6=8	8 marks
(2)	The two service feasibility testing by examination: diagram→2 marks Explanation : 6 points □ 6 marks → refer Text 1 Total= 2+6 =8	8 marks
	PART-2	
(3)	The relationship between sufficient and N&S feasibility test. Diagrams → 4 marks , explanation →4 marks Total= 4+4 =8	8 marks
(4)	Pseudo code outline of a basic service that polls an input interface for a specific input vector→5 marks, explanation→ 3marks Total= 5+3 =8	8 marks
	PART 3	
(5)	With two-service examples used derive RM LUB for case1: 6 steps with explanation →4 + 4 marks Total= 4+4=8	8 marks
(6)	An expression for RM LUB mathematically. 8 steps→ 8 marks Total= 8X1=8	8 marks

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	PART 4	
(7)	Two algorithms for determination of N&S feasibility testing with RM policy →4+4 Total= 4+4=8	**8 marks**
(8)	RM policy for overload scenario →4 marks cascading overload scenario → 4 marks Total= 4+4=8	**8 marks**
	PART 5	
(9)	The Worst-Case Execution Time (WCET) with relevant equation: equation and explanation → 2 + 6 marks Total= 2+6=8	**8 marks**
(10)	The overlapping definitions → 4 marks The overlapping conditions for CPU time →4 marks Total= 4+4=8	**8 marks**

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