

**P.E.S INSTITUTE OF TECHNOLOGY
 BANGALORE SOUTH CAMPUS
 DEPARTMENT OF E&C
 M.Tech in VLSI AND EMBEDDED SYSTEM
 SCHEME AND SOLUTION
 FIRST INTERNAL TEST**

Faculty: Ananda M
Subject: VLSI Testing

Semester : Second
Subject Code: 14EVE22

Q. No.	Note: Answer FIVE full questions, selecting any ONE full question from each part.	Marks
PART 1		
(1)	(a) Comparison between Verification and Testing: 4 points- 4marks → refer Slides (b) Pre-Silicon Validation and Post-Silicon Validation: 4 points- 4marks → refer slides <p align="center">Total= 4+4=8</p>	8 marks
(2)	(a) Real Defects in Chip: explain with example: 4 marks → refer slides (b) Two class of Non-Permanent class: Transient Fault → 2 marks, refer slides Intermittent Fault → 2marks, refer slides <p align="center">Total= 4+2+2=8</p>	8 marks
PART-2		
(3)	(a) (i) Role of Testing: Text 4:chapter3 → 2 marks (ii) Yield and Reject Rate: Text 4:chapter3 → 2 marks (b) Definitions (i) Failure (ii) Fault and (iii) Error in a Digital circuit: 1+1+2 → 4mark s <p align="center">Total= 2+2+1+1+2 =8</p>	8 marks
(4)	The Basic Testing Principle –diagram → 2 marks, explanation → 2marks The Infamous Design/Test Wall with -diagram → 2 marks → 2marks <p align="center">Total= 2+2+2+2 =8</p>	8 marks

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(5)	PART 3 The new VLSI Design Flow in Testing- diagram → 4 marks and explanation → 4 marks Total= 4+4=8	8 marks
(6)	Compare between Ideal Test and Real Test: any 6 points → 8 marks Total= 8	8 marks
(7)	PART 4 Fault Models are requirements: any 4 point → 4 marks and Mention all fault Models → 4 marks Total= 4+4=8	8 marks
(8)	The levels of Abstraction in Logic circuits- diagram → 3 marks Explanation → 5 marks Total= 3+5=8	8 marks
(9)	PART 5 (i) Functional Fault Models → 4 marks and (ii) Structural Fault Models → 4 marks Total= 4+4=8	8 marks
(10)	(i) Single stuck-at fault → 4 marks and (ii) Multiple Stuck at fault with examples → 4 marks Total= 4+4=8	8 marks