Question Bank for Analog and Digital electronics(15CS32)

Module 1: Field Effect transistors

1. Explain the working of CMOS, with its power consumption properties?

2. Explain construction and principle of operation of JFET along with its drain and trans-conductance characteristics?

3. Explain construction and principle of operation of D-MOSFET along with its drain and trans-conductance characteristics?

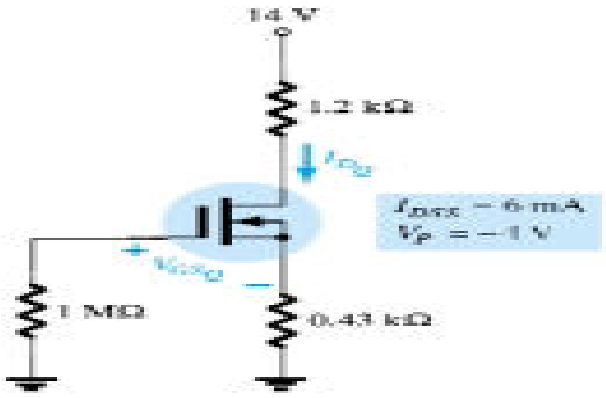
4. Explain construction and principle of operation of E-MOSFET along with its drain and trans-conductance characteristics?

5. Draw the cross-sectional view of an N channel JFET and explain its principle of operation, Draw the Ig vs Vds graph for different values of Vgs and highlight the different regions of operation.

6. Write the differences between JFETs and MOSFETs.

7. Draw the circuit for voltage divider configuration for E-MOSFET.
   a. Also derive the expression for the operating point.

8. For the self-bias configuration of Fig.2. Determine:
   (a) *IDQ* and *VGSQ*. (b) *VDS* and *VD*.

b. 

9. What is differences b/w ideal and practical op-amp amplifier?

10. With a neat diagram explain op-amp Schmitt Trigger circuit?

11. Explain astable multivibrator using 555 timer?

12. Explain mono multivibrator using 555 timer?

13. Explain Comparator? How do you convert sine wave to rectangular output, using Op-Amp?

14. Explain the CMRR, Slew rate, PSRR and gain-bandwidth performance parameter of a practical op-amp?

15. Define slew rate of Op–Amp. (ii) Determine the cutoff frequency of OP–amp whose unity gain bandwidth is 1 MHz and open loop gain is 2×10^5. (iii) List the expression for the output of non–inverting amplifier and inverting op-amp amplifier

16. What is an peak detector & absolute value circuit? Explain the functional principal, with the circuit?

17. Draw the circuit diagram of a current to voltage converter using opamps. What type of feedback is used in the circuit? What decides the maximum value of feedback resistance to be used in the circuit?

18. Draw the basic circuit of three op-amp instrumentation amplifier and explain its operation?

19. What is the main advantage of using a comparator with hysteresis over a conventional comparator? Explain with transfer characteristics?

20. What is a window comparator? Draw a circuit diagram of a window comparator that produces a low output for the input signal inside the window and high output for input outside the window.
21. What are the requirements of a good Instrumentation Amplifier?

22. What is an absolute value circuit? Explain the functional principal, with the circuit?

23. Draw the circuit diagrams, which introduce a phase-shift of 0 to -180 and 0 180 to 0 degrees for a sine wave input signal.

24. Draw the circuit diagram of a voltage follower. What are its closed loop voltage gain and bandwidth?

25. Distinguish between bistable ,monostable and astable multivibrators.

Module 2: The Basic Gates.

1. Explain the logic circuit and truth table of the Inverter, OR gat and AND Gate

2. Why NAND & NOR gates are called universal gates.

3. Differentiate between positive and negative logic.
4. Convert NAND gate into Inverter, in two different ways.
5. What are universal gates? Implement the following function using universal gate ((A+B) C)) D
6. Implement AB+CD with only three NAND gates. Draw logic diagram also. Assume the inverted input is available.
7. What is assertion level logic?
8. Explain Expander with an example.
9. Minimize the following using K-maps:
   i)SOP expression given by $f(A,B,C,D) = \Sigma\, m(0,1,2,3,5,9,14,15) + \Sigma\, \Phi(4,8,11,12)$
   ii)POS expression given by $f(A,B,C,D) = \Pi M(0,1,2,5,8,9,10)$
10. Implement the minimal expressions thus obtained using basic gates(both normal and inverted inputs can be used)
11. List out the difference between combinational and sequential logic circuits.
12. Demonstrate by means of Truth table the validity of following theorem of Boolean algebra.
    i) Associative law ii) Demorgan's law for Validity
    iii) Distributive law
13. Simplify the following Boolean function to minimum no. of literals.
    i) $xy+xy^1$ ii) $(x+y)_1(x+y^1)$
    iii) $xyz+x^1y+xyz^1$ iv) $y(wz^1+wz)+xy$
    v) $(A+B)^1\ ((A^1+B^1)^1$
14. Reduce the Boolean Expression to required number of literal.
    i) $BC+AC^1+AB+BCD$ ii) $[(CD^1) + A\ ]^1+A+CD+AB$
    iii) $[(A+C+D)\ (A+C+D^1)\ (A+C^1+D)\ (A+B^1)$
15. Obtain Truth table for function $F=xy+xy^1+y^1z$.
16. Convert the following to other canonical form.
    i) $F(x,y,z)=\sum(1,3,7)$
    ii) $F(A,B,C,D)=\sum(0,2,6,11,13,14)$
    iii) $F(x,y,z)=\Pi(0,1,2,3,4,6,12)$
17. Show that dual of Exclusive-OR is equal to its complement.
18. Expand the following function into canonical SOP form
    $f(x1,x2,x3) = x1x3 + x2x3 + x1x2x3$
19. Expand the following function into canonical POS form
    $F(W,X,Q) =(Q+W^1)\ (X+Q^1)(W+X+Q)\ (W^1+X^1)$

20. Mention different methods of simplifying Boolean functions.

21. Discuss K-map & Quine McCluskey methods for simplification Of Boolean expressions.

22. Define term Dont care condition.

23. Explain K-map representation in detail & discuss the merits & demerits.

24. Explain the tabulation procedure in detail & discuss merits & demerits.

25. Compare K-map & Quine - McClusky methods for simplification of Boolean Expression.

26. Obtain the simplified expression in sum of products For the following:
$F(A,B,C,D,E) = \sum(0,1,4,5,16,17,21,25,29)$

27. Obtain simplified expression in SOP & POS form
i) $x^1z^1+y^1z^1+yz^1+xyz$
ii) $^1yz^1+vw^1z^1+vw^1x+v^1wz+v^1w^1y^1z^1$

and draw gate implementation using AND & OR gates

28. Given the function $T(w,x,y,z)=\Sigma(1,3,4,5,7,8,9,11,14,15)$. Use K map to determine the set of all prime-implicants. Indicate essential prime-implicants, find three distinct minimal expressions for T

29. Using tabulation method, determine the set of all prime implicate for the function
$f(w,x,y,z) = \Sigma(0,1,2,5,7,8,9,10,13,15)$ and hence obtain the minimal form of given function, employing decimal notation.

30. Compare K-map & Quine-McCluskey methods for simplification of Boolean Expression. Give their merits and demerits.

31. Using K-map simplify following Boolean expression & give implementation of same using
i) NAND gates only
ii) AND, OR & Invert gates for
$F(A,B,C,D) = \sum(2,4,8,16,31) + \sum D(0,3,9,12,15,18)$

32. Simplify Boolean function by Tabulation method
$F(A,B,C,D,E,F,G) = \sum(20,28,52,60)$
$F(A,B,C,D,E,F,G) = \sum(20,28,38,39,52,60,102,103,127)$

33. Give two simplified irredundant expression for

F(w,x,y,z)= ∑(0,4,5,7,8,9,13,15)

34. Determine set of Prime implicants for function
F(w,x,y,z)= ∑(0,1,2,5,7,8,9,10,13,15)

35. Minimize the following function with don't care terms using Q.M. method
f(A,B,C,D)= m(5,7,11,12,27,29)+d(14,20,21,22,23)
f(A,B,C,D)= ∑m(1,4,6,9,14,17,22,27,28,)+d(12,15,20,30,31)

36. Determine the set of Prime-implicants for function
F(w,x,y,z)=∑(0,1,2,5,7,8,9,10,13,15)

37. Using Quine-Mc Clauskey obtain the set of Prime implicants for function F(a,b,c,d,e)= ∑(4,12,13,14,16,19,22,24,25,26,29,30)+ ∑d(1,3,5,20,27)

38. Prove the following Boolean identities:
1. A(B'+C)=AB'+AC
2. A(A+B'C)=A
3. A'B'+AB'+AB=A+B'

39. Find minimal sum and minimal product of the following Boolean function.
f(W,X,Y,Z)=∑m(0,1,3,7,8,12)+d c(5,10,13,14)

40. Using Quine McCluskey method, determine the prime applicants of the following function.
f(W,X,Y,Z)=∑m(7,9,12,13,14,15)+d c(4,11)

Module 2: Data Processing Circuits.

1. Why is a Multiplexer called a Universal logic circuit?

2. Configure 16 to 1 MUX using 4 to 1 MUX

3. Implement the f(x,y,z) = ∑m (0,4,5,6) function using 8 to 1 MUX

4. Implement the f(x,y,z) = ∑m (0,1,2,7) function using 4 to 1 MUX

5. Implemen the f(w,x,y,z) = ∑m (0,1,5,6,15,7,10,9) function using 8 to 1 MUX. Treat a, b and c as the select lines.

6. Implement the above using 4 to 1 MUX with a and b as select lines.

7. Implement the Boolean function
f(a,b,c,d) = ∑ m (4,5,7,8,10,12,15) using 4 to 2 MUX and external gates if, a and b are connected to select lines a1 and a2 respectively, c and d are connected to select lines a1 and a2 respectively.

8. Implement the following using 3 to 8 decoder with NAND outputs or active low outputs
F1(a,b,c) = ∑m(1,3,5,6); F2(a,b,c) = ∑m(0,2,5,6)

9. Define parity generator and parity checker.

10. Define an excess-3 to 8421 code converter using a 4 to 16 decoder with an enable input using NAND gates, so as to minimize the gate inputs.

11. Using decoder implement the following Logic functions.
a. Active High decoder with OR gate,
b. Active Low decoder with NAND gate,
c. Active High decoder with NOR gate,
d. Active Low decoder with AND gate.

12. Design 2-4 decoder with enable input E.

13. Design 3-8 decoder.

14. Design 4-16 decoder.

15. Mention the application of decoder.

16. How many outputs a magnitude comparator generates?

17. Show how two 1 to 16 demultiplexer can be connected to get 1 to 32 demultiplexer.

18. Design a 32 to 1 multiplexer using two 16 to 1 multiplexers and one 2 to 1 multiplexer.

19. Give seven segment decoder using PLA.

20. Show that using a 3-to-8 decoder and multi-input OR gate, the following expressions can be realized.
F1(A,B,C)= ∑m(0,4,6); F2(A,B,C)= ∑m(0,5);
F3(A,B,C)= ∑m(1,2,3,7)

21. Design Decimal to BCD encoder.

22. What are the different types of PLDs and implement the 7-segment decoder.

23. Mention different types of ROMS and explain each one of them.

24. What are the different models for writing a module body in Verilog HDL. Give an example for any one model.

25. Realize the Boolean expression $f(w,x,y,z) = \sum m(4,6,7,8,10,12,15)$ using 4:1 line mux and external gates.

Module 4: Flip-Flops

1. Mention the difference between combinational & sequential circuits with block diagram.

2. Mention the difference between asynchronous & synchronous circuits with example.

3. Differences between Latch & Flip flop give example.

4. Define clocked sequential circuit.

5. Difference between Characteristic & Excitation table.

6. Explain the operation of different types of flip flop.

7. What is Race around condition. Explain.

8. Explain the operation of JK flip-flop. With logic diagram, characteristic table.

9. Discuss how unstable condition S=R=1 is avoided in storage latch of the following:
   a) D latch b) JK flip flop c) T flip flop

10. Explain clocked RS flip flop with logic diagram.

11. Show that clocked D flip-flop can be reduced by one gate.

12. Explain how D & T flip flop works with logic diagram.

13. Discuss state table, state diagram, and state equation with example.

14. Explain what are registers?

15. Give a block diagram of sequential circuit employing register as a part of sequential circuit.

16. What are the applications of flip-flops?

17. How flip-flop will differ from latches?

18. Differentiate between combinational and sequential circuit.

19. Show how to convert a D flip flop into SR flip flop.

20. Explain the working of a JK Master- slave flip flop. Write its truth table state diagram and excitation table.

21. Show how to convert a SR flip flop into JK flip flop.

22. Mention the capabilities of shift register.

23. Explain universal shift register (74194).

24. Design synchronous BCD counter using JK flip flops.

25. Explain how shift register can be used as counters.

26. Mention the difference between ripple & synchronous counters.

27. Discuss shift registers.

28. Discuss state table, state diagram, and state equation with example.

29. Discuss the procedure for designing sequential circuits.

30. Define counter and write state diagram for 3-bit binary counter.

31. Explain registers.

32. Discuss serial transfer of information from one register to other.

33. Give a block diagram of sequential circuit employing register as a part of sequential circuit.

34. Give logic diagram of 4bit bi-directional shift register with parallel capability & briefly explain it's operation.

35. Give logic diagram of 4-bit ripple counter & BCD Ripple counter

36. Construct mod 6 counter using MSI chip.

37. Write the logic diagram of a 4bit bi-directional shift register with parallel load capability and explain its operations.

38. Design a 4-bit serial input shift registers in detail and give itstiming diagram.

39. Design a mod-5 synchronous up counter using JK flip flop.

40. Name and explain in short the four basic types of shift register and draw the block diagram for each.

Module 5: Counters

1. How many flip-flops are required to construct a mod-128 counter?
2. What is the largest decimal number that can be stored in a mod 64 Counter?
3. Differentiate between Synchronous and Asynchronous counter.
4. Write a Boolean expression for the And gate connected for the AND gate Connected to the lower leg of the OR gate that drives the clock input to Flip-flop QA in 54/74193.
5. Design a 4-bit ripple counter using negative edge triggered JK flip-flop.
6. Design a 4-bit binary ripple counter using positive edge triggered D-Flip Flop without a count enable line.
7. Design a mod-5 synchronous counter to sequence the first 5 state from 0000 to 0100 and repeat using a 4-bit synchronous counter with parallel load facility.
8. Explain 4-bit shift register of serial with timing diagram.
9. Explain ripple counter with truth table and waveform.
10. Design a divide by two counter using D-Latch.
11. Distinguish between a ring counter and Johnson counter.
12. Explain the working of a 3-bit asynchronous down counter.
13. Design an synchronous mod-5 up counter using JK flip flop.
14. Give excitation table. The counter sequence is 0,1,2,0,1

15.Find the binary weight of each bit in a 4-bit system.

16.What are the output voltages caused by each bit in a 5-bit ladder if the input levels are 0=0 v and 1 = +10v

17.How many bits are required in a binary ladder to achieve a resolution of 1 mV if full scale is +5V

18.Find the following for a 12-Bit counter type A/D converter using 1-MHz clock:

a. Maximum conversion time, b. Average conversion time

c. Maximum conversion rate.

19. What is the conversion time of a 12-bit section-counter-type A/D Converter using 1 – MHz clock? The counter is divided into three parts.

20. What is the resolution of a 9-bit D/A converter which uses 9 ladder networks? What is the resolution expressed as a percent? If the full-scale output voltage of this converter is +5v, what is the resolution in volts?

21. Explain with the block diagram of successive approximation ADC.

22. What is a binary ladder? Explain the binary ladder with digital input of 1000.

23. Explain accuracy and resolution for ADC.

24. Explain a 2-bit simultaneous A/D converter. Draw the block diagram of the same.

25. Explain continuous A/D converter with an example.