PESIT Bangalore South Campus

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Department of Computer Science and Engineering

ADVANCED COMPUTER ARCHITECTURE 10CS74

Question Bank

UNIT 1

1. Define Computer Architecture. Illustrate the seven dimensions of an ISA?

2. What is dependability? Explain the two measures of Dependability?

3. Give the following measurements
Frequency of FP operations=25%
Average CPI of other instructions=1.33
Average CPI of FP operations=4.0
Frequency of FPSQR=2%
CPI of FPSQR=20
Assume that the two design alternative are to decrease the CPI of FPSQR to 2 or to decrease the average CPI of all FP operations to 2.5 compare the two design alternatives using the processor performance equations.

4. Explain in brief measuring, reporting and summarizing performance of computer.

5. Explain with learning curve how the cost of processor varies with time along with factors influencing the cost.

6.Find the number of dies per 200 cm wafer of circular shape that is used to cut die that is 1.5 cm side and compare the number of dies produced on the same wafer if die is 1.25 cm.

7. Define Amdahl's law. Derive n expression for CPU clock as a function of instruction count, clocks per instruction and clock cycle time.

8. List and explain four important technologies, which has lead to improvements in computer system.

9. Define dependability and its measures. Assume a disk subsystem with the following Components and MTTF: 10 disks, each rated at 1,000,000-hour MTTF
1 SCSI controller, 500,000- hour MTTF
1 power supply, 200,000-hour MTTF
1 fan, 200,000-hour MTTF
1 SCSI cable, 500,000- hour MTTF
Assuming failures are independent, compute the MTTF of the system as a whole. Suppose we

Made the following measurements:
Frequency of FP operations = 25%
Average CPI of FP operations = 4.0
Average CPI of other instructions = 1.33
Frequency of FPSQR = 2%
CPI of FPSQR = 20
Assume that the two design alternatives are to decrease the CPI of FPSQR to 2 or to
Decrease the average CPI of all FP operations to 2.5. Compare these two design
Alternatives using processor performance equation.

10. We will run two application needs 80% of the resources and the other only 20% of the resources.
i>Given that 40% of the first application is parallelizable, how much speed up would you achieve with that application if run in isolation?
ii>given that 99%pf the second application is parallelized, how much speed up would this application observe if run in isolation?
iii> Given that 40% of the first application is parallelizable, how much overall speed up would you observe if you parallelized it?

UNIT 2

1. With a neat diagram explain the classic five stage pipeline for a RISC processor.

2. What are the major hurdles of pipelining? Illustrate the branch hazard in detail?

3 With a neat diagram explain the classic five stage pipeline for a RISC processor.

4. Explain how pipeline is implemented in MIPS.

5. Explain different techniques in reducing pipeline branch penalties.

6. What are the major hurdles of pipelining? Explain briefly.

7. List and explain five ways of classifying exception in a computer system.

8. List pipeline hazards. Explain any one in detail.

UNIT 3

1. What are the techniques used to reduce branch costs? Explain both static and dynamic branch prediction used for same?

2. With a neat diagram give the basic structure of tomasulo based MIPS FP unit and explain the various field of reservation stations.

3. What are data dependencies? Explain name dependencies with examples between two instructions.

4. What are correlating predictors? Explain with examples.

5. For the following instructions, using dynamic scheduling show the status of R.O.B, reservation station when only MUL.D is ready to commit and two L.D committed.
L.D F6, 32 (R2)
L.D F2, 44(R3)
MUL.D F0, F2, F4
SUB.D F8, F2, F6
DIV.D F10,F0,F6
ADD.D F6,F8,F2
Also show the types of hazards between instructions.

6. What is the drawback of 1- bit dynamic branch prediction method? Clearly state how it is overcome in 2- bit prediction. Give the state transition diagram of 2-bit predictor.

UNIT 4

1. Explain the basic VLIW approach for exploiting ILP using multiple issues?

2. What are the key issues in implementing advanced speculation techniques?
Explain them in detail?

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Explain in detail?

4 .Write a note on value predictors.

5. Explain branch-target buffer.

6. Write a short note on value predictor.

7. What are the key issues in implementing advanced speculation techniques?
Explain them in detail?

UNIT 5

1. Explain the basic schemes for enforcing coherence in a shared memory multiprocessor system?

2. Explain the directory based coherence for a distributed memory multiprocessor system?

3. Explain the directory based cache coherence for a distributed memory multiprocessor system along with state transition diagram.

4. Explain any two hardware primitive to implement synchronization with example.

5. List and explain any three hardware primitives to implement synchronization.

6. Explain the directory based coherence for a distributed memory multiprocessor system?

UNIT 6

1. Assume we have a computer where the clock per instruction (CPI) is 1.0 when all memory accesses hit the cache. The only data accesses are loads and stores and these total 50 % of the instructions. If the mass penality is 25 clock cycles and the mass rate is 2%.how much faster would the computer be if all instructions were cache hits?

2. Explain in brief, the types of basic cache optimization?

3. Explain block replacement strategies to replace a block, with example when a cache.

4. Explain the types of basic cache optimization.

5. With a diagram, explain organization of data cache in the opteron microprocessor.

6. Assume we have a computer where CPI is 1.0 when all memory accesses hits in the cache. The only data accesses are loads and stores, and these 50% of the instruction. If the miss penalty is of 25 cycles and miss rate is 2%, how much faster the computer be, if all the instruction were cache hits?

7. Briefly explain four basic cache optimization methods

UNIT 7

1. Which are the major categories of the advanced optimization of cache performance? Explain any one in detail.

2. Explain in detail the architecture support for protecting processes from each other via virtual memory

3. Explain the following advanced optimization of cache:
1.) Compiler optimizations to reduce miss rate.
2.) Merging write buffer to reduce miss penalty.
3.) Non blocking cache to increase cache band-width

4. Explain internal organization of 64 Mb DRAM.

UNIT 8

1. Explain in detail the hardware support for preserving exception behavior during Speculation.

2. Explain the prediction and Speculation support provided in IA64?

3. Explain in detail the hardware support for preserving exception behavior during Speculation.

4. Explain the architecture of IA64 Intel processor and also the prediction and Speculation support provided.

5. Consider the loop below:

```
For ( i = 1;i ≤ 100 ; i = i+1 {
A[ i ]= A[i] + B[i] ; 1 * S1 *1
B[ i+1]= C[i] + D[i] ; 1 * S2 *1
}
```

What are the dependencies between S1 and S2? Is the loop parallel? If not show How to make it parallel.